LCD DRIVER

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BACKGROUND OF THE INVENTION

[0001] This application claims the benefit of Provisional Application No. 60/416,855 filed October 8, 2002 which is incorporated herein by reference in its entirety.

[0002] This invention relates in general to liquid crystal displays (LCDs) and, in particular, to an LCD driver.

[0003] Fig. 1 is a schematic view of a LCD panel and its n row electrodes labeled COM 1, ...COM n in Fig. 1, and k column electrodes shown as vertical rectangles labeled SEG 1~SEGk in Fig. 1. Not shown in Fig. 1 (to simplify the figure) is a layer of liquid crystal material between the row and column electrodes. When an appropriate voltage is applied across a particular row and a particular column electrode, a portion of the liquid crystal layer between the particular row and column electrodes where they overlap controls the light transmission or reflective properties of such portion, where the overlapping portion of each row and each column electrode when viewed in a viewing direction defines a pixel of the LCD panel.

[0004] Fig. 2a is a graphical illustration of the Improved Alto-Pleshko (IAPT) waveform for the row (or COM) electrodes and column (or SEG) electrodes. Fig. 2b is a graphical plot of the conventional Alto-Pleshko driving waveform for row (COM) and column (SEG) electrodes. In Figs. 2a and 2b, voltages labeled V_{COM} or variations thereof indicate voltage waveforms that are applied to the row electrodes and voltages labeled V_{SEG} or variations thereof indicate voltage waveforms applied to column electrodes. The driving waveforms in Figs. 2a and 2b are conventional. Referring to Fig. 1 and Fig. 2a, a typical configuration of passive LCD and a conventional driving waveform are illustrated. As demonstrated in Fig. 1, the ith row electrode is connected to a node at voltage V_{COMi}, on one side, and the jth column electrode is connected to a node at voltage V_{SEGj} on the other side. In Fig. 2a, where vertical axis is voltage, and the horizontal axis time, the data signals V_{SEGj} are also drawn as overlapped shaded region over V_{COMi} signal to illustrate relative relationships between these two sets of signals.

[0005] The driving waveform demonstrated in Fig 2a, is known as Improved Alto-Pleshko driving method (Improved APT, or IAPT for brief). The main characteristic is that the COM scanning pulses are "folded" such that the driving total voltage dynamic range is reduced as compared to the plain APT, as show in Fig. 2b. This reduced voltage range is considered to be advantageous in the conventional design technique used in CMOS integrated driver IC, where low MOS transistor break down voltage (caused by thin gate oxide used in fine gate geometry circuits and devices) would otherwise make the circuit design very difficult.

[0006] As shown in Fig. 2a, in field 2xN, the voltage that is supplied to the node V_{COMi} that is not being scanned is at V_5, and that applied to the row electrode that is scanned is at voltage V_1. During such field, the column or SEG electrodes are at V_6 or at V_4, depending on the data that is being applied to the column electrodes. In the field 2xN+1, the non-scanning voltage applied to the row electrodes is V_2, and the voltage applied to the row electrode that is being scanned is V_6. In such field, the voltages that are applied to the column or SEG electrodes are at V_0 or V_2, depending on the data that is being applied to such electrodes.

[0007] Thus, from the above, in the IAPT driving method, a total of six different electrical potentials are applied to the row and column electrodes. In the conventional APT driving method shown in Fig. 2b, it will be observed that a total of five different electrical potentials are applied (V_{COM+}, V_{B+}, V0, V_{B-} and V_{COM-}).

[0008] Fig. 2c is the graphical illustration of a portion of the IAPT driving waveform of Fig. 2a.

[0009] In order to provide the six different electrical potentials used in the IAPT waveform, or the five different electrical potentials used in the APT waveform, it has been found that the provision of two different electrical voltages, V_{LCD} and V_B, relative to ground are adequate. The way in which the six different electrical potentials used in the IAPT waveform may be generated by the provision of two different electrical voltages, V_{LCD} and V_B is described in U.S. patent application Serial No. 09/842,988, filed April 26, 2001, which is incorporated hereby in its entirety by reference. Thus, in one conventional LCD driver, a voltage divider is used which includes a number of resistors forming a ladder connected between two nodes at different electrical potentials.

[0010] One drawback of such a circuit is that a constant current flows through the power supply and causes constant power dissipation. One of the most frequently heard complaints from users of portable devices, such as portable computers, cellular phones and personal digital assistants is that these devices consume too much power so that one has to constantly charge batteries, which is inconvenient. It is therefore desirable to provide LCD drivers that consume less power in order to extend the battery life. This will be useful for all LCD drivers, and especially for LCDs used in portable devices. To decrease the current consumption in the conventional resistor ladder approach, the only way is to increase the resistance value of the resistors. But this has a negative effect of increasing chip die size. Thus a different approach is desirable.

SUMMARY OF THE INVENTION

[0011] This invention is based on the recognition that power consumption by the LCD driver can be reduced if a capacitor divider comprising a plurality of capacitors is used to provide one or more voltage level(s) and power for driving the LCD. In one embodiment, the capacitor divider comprises a plurality of capacitors that are electrically connected. The capacitor divider may be employed to provide IAPT as well as APT voltage levels or other driving waveform levels. In one embodiment, the control device such as one comprising one or more switches may be employed to connect the divider to row and column electrodes of an LCD to provide suitable voltage levels for driving the electrodes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Fig. 1 is a schematic view of an LCD panel and its row electrodes shown as shaded, horizontal rectangles labeled COM1, ... COMn and column electrodes shown as vertical rectangles labeled SEG1, ... SEGk useful for illustrating the invention.

[0013] Fig. 2a is a graphical illustration of the conventional improved AltoPleshko (IAPT) waveform for the row or COM electrodes and column or SEG electrodes.

[0014] Fig. 2b is a graphical plot of the conventional Alto-Pleshko driving waveform for row (COM) and column (SEG) electrodes.

[0015] Fig. 2c is a graphical plot of a portion of the IAPT driving waveform of Fig. 2a.

[0016] Fig. 3 is a schematic view of a capacitor divider circuit to illustrate one embodiment of the invention.

[0017] Fig. 4 is a schematic view of the capacitor divider circuit with periodic refreshing feature to illustrate another embodiment of the invention.

[0018] Figs. 5a and 5b illustrate two different phases of a capacitor divider to illustrate another embodiment of the invention.

[0019] Fig. 6 is a schematic circuit diagram of a capacitor divider circuit for implementing the two phases of operation shown in Figs. 5a and 5b.

[0020] Fig. 7 is a schematic circuit diagram of a capacitor divider to illustrate still another embodiment of the invention.

[0021] Fig. 8 is a schematic circuit diagram of a capacitor divider to illustrate one more embodiment of the invention.

[0022] Fig. 9 is a schematic view of a capacitor divider to illustrate yet another embodiment of the invention.

[0023] Fig. 10 is a graphical plot illustrating electrical potentials for driving an LCD display that comprises three row electrodes R1, R2 and R3, and two column electrodes C1 and C2.

[0024] For simplicity in description, identical components are labeled by the same numerals in this application.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0025] The ratio of V_{LCD} over V_B in Fig. 2c is defined as a parameter called bias ratio. Instead of a resistor ladder as used conventionally, a capacitor divider circuit 10 can be employed to generate the bias ratio and to provide the electrical potentials V_{LCD} and V_B of Fig. 2c as shown in Fig. 3. The bias ratio BR is

$$BR = \frac{C_2 + C_1}{C_1} \qquad \text{Eg. 2}$$

, where C_1 and C_2 are values of the top capacitor 12 and bottom capacitor 14 in Fig. 3.

[0026] Since no static current is required to drive the capacitor divider 10, power is saved through this approach.

[0027] One drawback of this approach is that the node A between two capacitors is a floating node (i.e. at a floating electrical potential). Its initial voltage is undetermined. Also over long period of time, the voltage may tend to drift because of capacitor leakage current. These two factors will affect the voltage value at node A.

[0028] These two problems are solved by a periodic refreshing circuitry in the capacitor divider 20 as shown in Fig. 4. Three switches S_1, S_2 and S_3 are added to the divider to form an enhanced capacitor divider circuit 20. On clock phase 1, switches S_1 and S_2 are closed and switch S_3 is open. All capacitor terminals are reset to ground and the charges on capacitors 12 and 14 are cleared. On clock phase 2, switches S_1 and S_2 are open and switch S_1 is closed. In this phase, the capacitor circuit 20 can divide the voltage levels accurately and consistently.

Power Saving

[0029] Through the use of capacitor dividers, substantially no static current will be passing through the divider circuit. Only the periodic refreshing of these capacitors in the manner described above can cause dynamic power consumption. A typical example will be that refreshing frequency is 80 Hz, V_{LCD} = 10 V, C_1 = 10 pF, C_2 = 90 pF. Then the current consumption is

$$I = V_{LCD} * f * C_1 * C_2/(C_1 + C_2) = 7.2nA \qquad \text{Eq.3}$$

[0030] In the conventional resistor divider approach, where the same V_{LCD} at 10V is divided by the total resistance of 1 Mohm of resistors, the total current would be 10 μA. The power saving of the embodiment in Fig. 4 compared to the conventional resistor divider approach is more than 1000 times.

[0031] An alternative circuit is available to generate the bias ratio as shown in Figs. 5a and 5b which illustrate two different phases of a capacitor divider to illustrate another embodiment of the invention. In this circuit, an array of capacitors 40 of substantially equal value is employed. The number of capacitors is preferably equal to the bias ratio. In clock phase 1 (not shown), the capacitors are connected in series between V_{LCD} and ground, so each capacitor has a V_{LCD}/N voltage drop, where N is the number of

capacitors in the array. In this phase, the capacitors connected in series into a capacitor divider is used to provide electrical potentials for driving a LCD. In clock phase 2 (not shown), the capacitors are connected in parallel and to a power source for charging the capacitors. When N is selected to be bias ratio, a proper V_B voltage is generated for LCD driver.

[0032] The circuit illustrated in Figs. 5a and 5b is particularly useful when the bias ratio is low, e.g. 3 or 4. A small number of capacitors can generate the bias ratio effectively with very little power consumption.

[0033] Fig.6 shows the detailed implementation of the circuit 50 whose operation is illustrated in Figs. 5a and 5b. In phase 1, all the S1 switches are closed so that the capacitors 40 are connected in series. In phase 2, all the S2 switches are closed. The capacitors are then connected in parallel to generate V_B.

[0034] Fig. 7 shows the connection between the capacitor divider and four nodes V_{COM_SCAN}, $V_{COM\_NONSCAN}$, V_{SEG0} and V_{SEG1} in a LCD COM/SEG circuit. As will be evident from Figs. 7 and 2a, when the switches S_1 are closed in Fig. 7 in one phase of operation, the voltage waveforms in field 2xN shown in Fig. 2a will be generated. Where switches S_2 are closed instead in another phase of operation, however, the voltage waveforms of field 2xN+1 will be generated instead.

[0035] From Fig. 2a, it will be observed that a total of six electrical potential levels have been generated: V_1 through V_6. Instead of generating six different electrical potentials, IAPT voltage waveforms having shapes similar to those of Fig. 2a can be generated by means of a capacitor divider comprising four capacitors instead of five, as illustrated in Fig. 8. Thus, instead of the six electrical potentials of Figs. 2a and 7, these six electrical potentials can be collapsed so that there is no voltage gap between the two intermediate electrical potentials (V_3 and V_4 of Fig. 2a) to arrive at the same potential V_3' and V_4' at the same potential illustrated in Fig. 8. Then voltage waveforms analogous to those of Fig. 2a will be generated by means of the capacitor divider of Fig. 8, but where the two intermediate voltages have now been collapsed into a single electrical potential. Consequently, the voltage waveforms generated will only be at five different electrical potentials instead of six. Therefore, where switches S_1 are closed in one phase of operation, a voltage waveform somewhat similar to that shown in Fig. 2a for the field

2xN will be generated. And when the switches S_2 are closed instead in another phase of operation, a voltage waveform somewhat similar to those in field 2xN+1 would be generated instead.

[0036] The five electrical potentials or voltage levels reached in the embodiment of Fig. 8 can be further compressed, so that in reference to the voltage levels in Fig. 2a, so that V_2 and V_4 are substantially at the same voltage level, and V_3 and V_5 are also substantially at the same voltage level. In such instance, the four voltage levels would be V_1, (V_2,V_4), (V_3,V_5) and V_6. These four voltage levels or electrical potentials have now been relabeled V0', V1', V2' and V_{LCD} as shown in Fig. 9. Therefore, as before, where switches S_1 are closed in one phase of operation, a voltage waveform somewhat similar to that shown in Fig. 2a for the field 2xN will be generated. And when the switches S_2 are closed instead in another phase of operation, a voltage waveform somewhat similar to those in field 2xN+1 would be generated instead.

[0037] Instead of using the capacitor divider 202 in the manner illustrated in Fig. 9, such divider can also be used for driving the row and column electrodes in a manner quite different from that shown in Fig. 2a. This is illustrated in Fig. 10. Especially where the LCD comprises a small number of row electrodes, the LCD driving waveform of Fig. 10 may be particularly advantageous. This may be useful in applications where small size screen LCDs will be adequate, such as watches, meters, instruments, clocks and other applications. Fig. 10 illustrates electrical potentials for driving an LCD display (not shown but of a similar construction as that in Fig. 1) that comprises three row electrodes R1, R2 and R3, and two column electrodes C1 and C2. The LCD driver 202 is used to provide the same four different electrical potentials as those in Fig. 9 to the row and column electrodes of the LCD. In order for a particular pixel to be turned on in the LCD, the electrical potential or voltage across the overlapping column and row electrode defining such pixel is V_{LCD}-V0'. If the electrical potential between or voltage across the overlapping column and row electrodes is less than such value, then this value would be inadequate to turn on the pixel. Each row is scanned for a time t shown in Fig. 10. Thus, for a row electrode that has been selected for scanning, the voltage applied to such selected row electrode would toggle between V0' and V_{LCD}, whereas the electrical potentials applied to the row electrodes that have not been selected would toggle between V1' and V2'. The electrical potentials applied to the column electrodes would also toggle

between V0' and V_{LCD} if on and toggle between V1' and V2' if off. Thus, according to the waveforms shown in Fig. 10, the voltage across only one pixel is adequate to turn on such pixel, namely, the pixel where row electrode R2 and column electrode C1 overlap.

[0038] Thus, from the above, it will be noted that the capacitor divider may include two, three, four, five or more capacitors in the divider. Such dividers may be employed and configured in different ways for supplying various voltage waveforms and power for driving LCDs.

[0039] While the invention has been described above by reference to various embodiments, it will be understood that changes and modifications may be made without departing from the scope of the invention, which is to be defined only by the appended claims and their equivalent. All references referred to herein are incorporated by reference in their entireties.